

OVERVIEW

In January of 2006, Technologic Systems and a customer jointly commissioned a professional and independent HALT test (Highly Accelerated Life Testing) for the TS-7250 single board computer design.

The goal of HALT testing is to break the product in order to reveal design weaknesses, but testers were unable to destroy a single off-the-shelf TS-7250. This article provides some general information about HALT testing and outlines the details of the TS-7250 HALT test.

INTRODUCTION

One of the most critical competition factors in the embedded systems market is the reliability of an embedded application, given that the simplest system failure may stop entire factory assembly lines or other expensive processes. In the same line, military and medical systems in particular are intolerant of failures, as lives may depend on the reliable functioning of equipment. In industrial or scientific applications, embedded systems may be outside the reach of humans, making failures costly in terms of down time of the system and the human labor involved in getting to the board.

Therefore, embedded computers must be designed to run continuously for years without errors, often in hostile environments that no desktop PC could endure. To meet these higher quality requirements of the industry and consumer market, it is required sophisticated testing processes and new performance evaluation techniques which provide a company the capability to figure how their design would hold up over the years, without having to wait that long.

Highly Accelerated Life Testing, or HALT, is a time compression testing protocol that utilizes a step stress approach in subjecting products to varied thermal and vibration stresses. It is used to uncover design limitations and weaknesses in the preliminary design phase, helping designers of embedded systems to find and fix errors before they occur in the field

The goal of HALT testing is to break the product by subjecting the test unit to progressively higher stress levels, incorporating thermal dwells, rapid temperature transitions, varied vibration stresses, and a combination of temperature and vibration to precipitate inherent defects. Through this intense stress, long term failure modes that would show up under normal operating conditions in months or years can be revealed in just hours or days.

Moreover, some typical problems that occur during the various stress test cycles include circuit design issues; intermittent, failed, degraded or cracked components; cold or insufficient solder joints; broken leads; screws that back out; socket failures; detached wires; and other failures that may reveal potential design weaknesses. Stressing the product to failure allows designers to assess design ruggedness and margin above its intended operation.

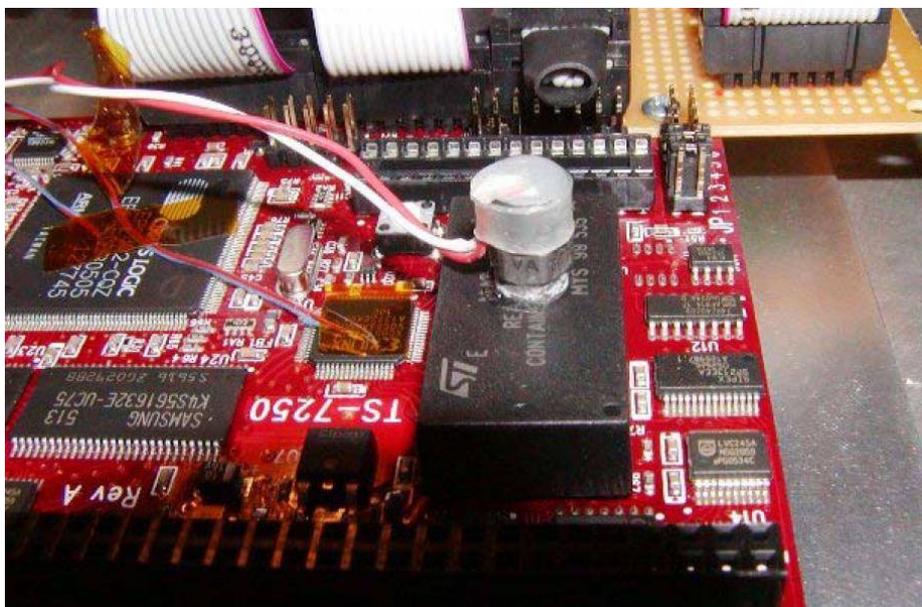
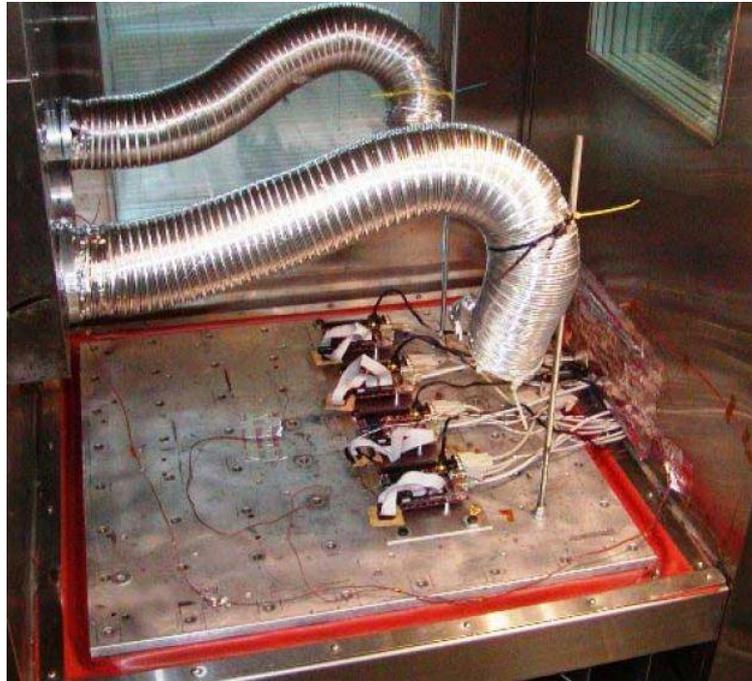
In general, HALT testing can provide engineers the information they need to improve designs before products fail in the field. Used properly, it can save money and time in the design phase of a product as well as increasing the reliability and profitability in resulting products. The HALT testing pushes a product past its limits so that engineers can see where and when failures occur, ensuring the overall ruggedness of the test product through more appropriate techniques of project and design.

HALT IN ACTION

In order to evaluate the performance of the Technologic Systems Single Board Computers (SBCs) under stress conditions and the typical hostile industrial environments which the embedded systems are subjected, four TS-7250 RevA units were submitted to the HALT process, realized by the OPS A La Carte LLC specialized partner (www.opsalacarte.com).

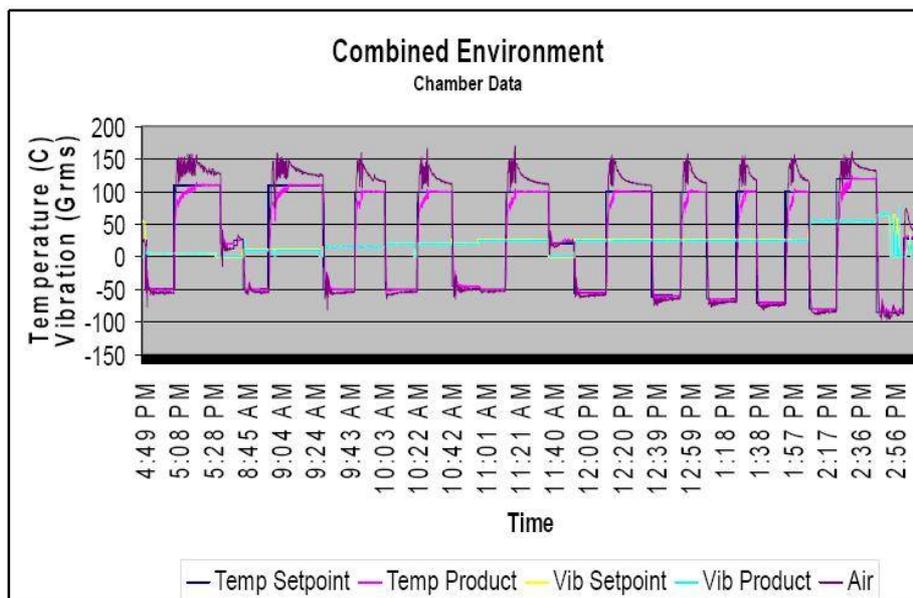
High precision measurement equipment was used to perform the test, such as thermocouples, a spectrum analyzer, accelerometers, a data acquisition interface and a signal conditioner.

The testing setup inside the HALT chamber is shown in the picture to the right. Also, a mounted board is shown below with placement measurement equipment, such as the accelerometer:



With the testing equipment all in place, the four TS-7250 boards were subjected to stress conditions using repeatable testing techniques such as thermal step stress, rapid thermal transitions, vibration step stress and combined temperature and vibration environments. These testing cycles create conditions that quickly reveal weaknesses in the product design and failure modes.

One good example which demonstrates the high stress conditions achieved by the HALT process is the combined temperature and vibration cycle. According to the official HALT report, during the test, the testing unit was exposed to 10 ½ rapid temperature cycles starting at -50oC to +110oC and ending at -85oC and +120oC. The vibration level is set to 5 Grms for the first temperature cycle and then increased in 5 Grms increments before each additional cycle through the cycle 5. For cycles 6 through 11, vibration levels started at 25 Grms and ended at 65 Grms. The dwell time at each temperature extreme was 10 minutes and the thermal transition rate was set to the chamber maximum (> 60oC/min. empty table). The graphic below illustrates how the temperature and vibration varied over time inside the testing chamber:



The HALT test quickly determined that the real world operating and destruct limits of the TS-7250 are well outside the stated operating temperature range of -20° to +70°C . In the context of this HALT test, the operating limit is defined as the last operational temperature or vibration set point to failure, while the destruct limit is the level at which the product stops functioning and remains inoperable at normal operating conditions. The table below shows the impressive results reached by off-the-shelf Technologic Systems boards:

Stress Condition	Operation Limit	Destructive Limit
Cold Temperature	-50oC (-58F)	-60oC (-76F)
Hot Temperature	+110oC (230F)	>+120oC (248F)
Vibration	25Grms	>55Grms

ENGINEERING ANALYSIS

Analysis done by Technologic Systems engineers and HALT test operators result in interesting conclusions and highlights, including:

- ✓ Even though the intention of the HALT test was to test the boards until they broke, testers were unable to destroy a single TS-7250. Actually, testers reported that the vibration table used in the testing started malfunctioning before anything on the board did.
- ✓ A +70oC rated TS-7250 board actually continues to work properly from -60oC(-76F) to +110oC (230F). At the high end temperatures, the epoxy inside the null modem cable started melting and seeping out yet the board continued to run fine. At the low end temperatures frost and snow was forming on the board. These temperatures were where the boards started exhibiting strange behaviors. Once the temperature was brought back down between -60oC and 110oC, the boards snapped back to life without any permanent damage.
- ✓ Boards still held together at 55 Grms. However, in a extreme high vibration environment, power connections need to be soldered down and loctite should be used on any DB9 screws, since they have a tendency to unscrew at extreme G force ratings. USB is not an industrialized connector and shouldn't be used in high vibration environments.
- ✓ The fast temperature cycles caused no problems. This is quite surprising as this is one of the most brutal things you can do to a board. Keeping the number of passive devices to a minimum and hand-routing the traces on the board paid off here.

IN CONCLUSION

The HALT test proved what our engineers and customers have long known - Technologic Systems products are built with quality and reliability in mind. You can feel secure incorporating Technologic Systems single board computers into your embedded system design.

If you would like to read the details of the HALT test with the TS-7250 boards, please refer to the **official test report** provided by the OPS A La Carte LLC.

CONTACT TECHNOLOGIC SYSTEMS

Technologic Systems builds rugged computers because we know how important reliability and longevity is to embedded applications. The internal electronics of our product are very simple to manufacture and operate with huge margins all around, using fewer layers, vias, chips, solder points and less exotic manufacturing technologies. If your embedded system is designed into medical, safety or security equipment, demand reliability in the hardware you choose.



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